Singaporean Journal of Scientific Research(SJSR)
Journal of Selected Areas in Microelectronics (JSAM)
Vol.8.No.2 2016 Pp.108-114
available at :www.iaaet.org/sjsr
Paper Received : 08-03-2016
Paper Accepted: 19-04-2016
Paper Reviewed by: 1.Prof. Cheng Yu 2. Dr.M. Akshay Kumar
Editor : Dr. Chu Lio

A LOAD ADAPTIVE ZVS AUXILIARY CIRCUIT FOR PWM DC-DC BUCK CONVERTER

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ABSTRACT

In this paper a soft switching ZVS dc dc converter is proposed to maximize the efficiency and to minimize the voltage stress across the switches. The PWM DC-DC converters convert high dc voltage at the output of a three-phase ac-dc converter to an isolated dc output voltage. DC-DC converters need high efficiency requirements at low and mid loads with high switching frequencies and it can be achieved by reducing switching losses. In the proposed system the DC-DC Converter meet the energy star platinum efficiency standard.

Index terms: Zero voltage switching (ZVS), DC-DC Converter, and Coupled Inductor.

1. INTRODUCTION

When the DC input voltage is higher than 500v, the dc-dc converters are used for galvanic isolation.[1]-[6] In High voltage applications the input DC voltage is split equally So that the peak voltage stress of the MOSFETs gets reduces and the dc bus capacitors are reduced to half of the input voltage. Compared to high voltage rated devices the low voltage rated semiconductor devices (MOSFETs) are used with optimized on-state resistance and with lesser parasitic components across the drain-source capacitance of MOSFETs. Recently high efficiency the three level dc-dc converters are used in telecommunication devices and datacenters power units.

At high switching frequencies the MOSFETs operate with zero voltage switching for improving the efficiency and providing the reliable operation of the dc-dc converter from no load to full load operation. To reduce the overall Electromagnetic Interference the converter operates from no load to the full load

and it leads to size and weight reduction of the EMI filter components which constitutes to the converter weight and volume. For high current applications, the current stress across the transformer and diodes are get reduced due to this the output performance will be better.

The pulse width modulated (PWM) scheme and soft switching technique Zero voltage switching have been proposed in three level dc-dc converters. The output capacitance and leakage impedance of the transformer are resonant. All switches should be turned on with ZVS operation.

2. CONVENTIONAL METHODS OF DC-DC CONVERTER

i) ZCS and ZCZVS PWM Three Level DC-DC Converters.

In IGBT's the Zero current switching reduces the switching losses but in MOSFETs the Zero voltage switching have been used [2]. To operate the frequencies less than the 100 KHZ the converters are either operated with only IGBTs or combination of IGBT and MOSFETs and it leads to very low power density. And these converters needs additional complex auxiliary circuits for realizing soft switching, but soft switching at no load or low loads are not guaranteed.

ii) PWM DC–DC Three-Level Converters With Entire Load Range Capability.

At higher loads the PWM dc-dc converters can have natural ZVS some of the methods which can achieve ZVS at no load fail to realize load adaptive ZVS over the full load range. The methods are as follows as A full range soft switching three-level converters were proposed in [1] based on auxiliary circuits with inductors connected to the middle nodes of the three-level converters to the dc bus splitting capacitors and flying capacitors. To create ZVS for full range the ramp current in the inductors are used. The drawback is that the ramp current remains constant over the entire load range the energy in the leakage inductor can be obtained at higher loads. Thus, these converters fail to obtain Load adaptive ZVS.

The high amount of current inductive arises at high loads from the constant current peaks of the external inductors can cause very fast discharge of the MOSFETs and reverse polarity charging occurs if the body diode of the MOSFET is not fast enough, which can lead to failure of the device.

Regarding turn-on characteristics the MOSFETs body diode is a slow device. If the converter is implemented with transformers connected in series magnetizing currents of transformers can be utilized for ZVS of the three-level devices. The ZVS range at low loads has been extended, but it suffers from some disadvantages:

During charging of the magnetizing inductor, the loss of duty ratio of the converter also increases the circulating current at mid and high loads. This results in severe restrictions of load range of the converter and efficiency loss at mid and high loads.

3. PROPOSED ZVS PWM DC DC CONVERTER

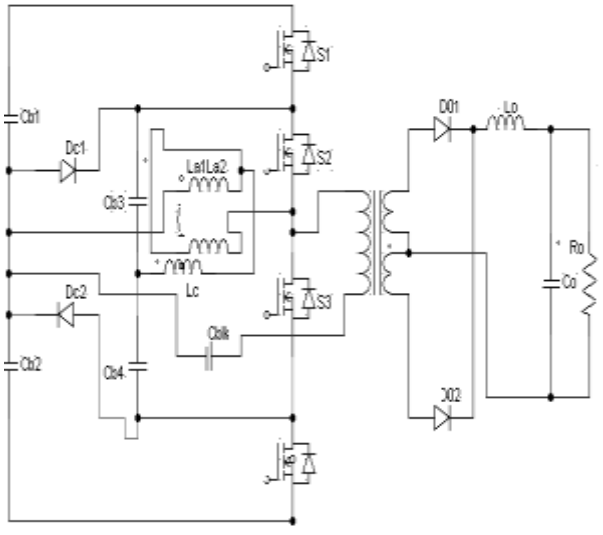

Figure 1.Proposed system of DC-DC converter

The proposed system of DC-DC converter has been shown in figure 1. To overcome the above drawbacks, a new converter topology was proposed using three level dc-dc converter. It comprises of auxiliary inductors La1 and La2 and dc bus-splitting capacitors Cb1, Cb2 to split the dc voltage, and flying capacitors Cb3 and Cb4 to increase the voltage which is also involved to balance the voltage along with clamping diodes Dc1 and Dc2. The auxiliary windings La1 and La2 have coupled the turns ratio of 1:1 and inductance of LC are the key components of the auxiliary circuit.

Some of the key objectives of this new auxiliary circuit are as follows:

1) Create an external current source to charge and discharge the coupled inductors which will be utilized for ZVS of the bridge devices from no-load to full load operation;
2) The current in the ramp lowers instantly with increasing load due to its magnetic coupling thus which is essential for reducing conduction losses from the Circulating currents and also optimize ZVS of the devices.

The phase shift control method is used to control the converter, the maximum duty cycle is 50% which means that duty ratio of each switch is 0.5 with some dead time; the gating pulses of switches S2 and S3 are complimentary, while those of S1 and S4 are complimentary with certain phase shift between the gating pulses of S2 and S3, respectively. It is this phase shift that defines duty ratio of the transformer primary voltage Vab and in turn, controls the output voltage.

The clamping diodes D−c1 and D−c2 are provided to equalize the voltage across the semiconductor devices and to clamp the voltage Vab to zero whenever necessary. The coupled inductor is modeled as an ideal transformer with two windings La1,La2 and turns ratio will be 1:1 with magnetizing inductance Lc. In this context, when the potential of its dotted end is greater than that of its other end. Current in the transformer primary is positive when it flows from node a to node. And when the potential of its dotted end is lesser than the other end the current in the transformer primary is negative.

At any time instance, the following relation holds well for the coupled inductor:

$iL_{a1} = -iL_C/2$ and $iL_{a2} = +iL_c/2$ (i)

The steady-state voltages Vcb3 and Vcb4 across the capacitors Cb3 and Cb4 should be +VDC/4. Due to the symmetrical operation of the converter over each half of the switching cycle, only the operation of the converter during half a switching cycle is discussed in this section.

SOFT SWITCHING TECHNIQUES

The problems of switching losses and EMI associated with hard-switching converter operation can be reduced by using soft-switching. The term "soft-switching" in power electronics refers to various techniques where the switching transitions are made to be more gradual to force either the voltage or current to be zero while the switching transition to be made. EMI is reduced by soft-switching because the switching transitions from on to off, and vice versa are gradual and not sudden. Switching losses are reduced since the power dissipated in a switch while a switching transition made is proportional to the overlap of the voltage across the switch and the current flowing through it.

Soft-switching forces either the voltage or the current to be absolutely zero during the time of transition; therefore there is no overlap between voltage and current and (ideally) no switching loss.

3. ANALYSIS OF PROPOSED DC-DC CONVERTER

i).ZVS Condition for Switch Pair S1, S4.

The ZVS condition for the outer switch pair S1, S4 is different from that of the inner switch pair S2, S3 due to the involvement of the output inductor during the switching instances of S1 andS4.

Vdc/2=[(ilk(t1)+iaux1(t1)/CDS)]TD (ii)

The value of the leakage inductance is kept so low to reduce loss of duty cycle described in the modes of operation and also to reduce the peak voltage stress across secondary side rectifier [5]. It needs to be noted that the switch capacitance is highly nonlinear and is a function of the MOSFET drain-to-source voltage, the nonlinearity is especially prominent at voltages of 200 V and less, so it has to be accurately evaluated from the characteristic log- linear graph of COSS versus VDS in the of the MOSFET.

ii).ZVS Condition for Switch Pair S2, S3.

The zero-voltage switching of the switches S2 and S3 are More critical than those of S1 and S4, since during the switching transitions of these switches there is no involvement of the larger output filter inductor reflected to the primary side of the transformer .Assuming that the auxiliary inductor is much larger than the leakage inductor so that it maintains a constant current during the switching instance of the devices S2, S3.

5. SIMULATION RESULTS

The simulation of the proposed system can be done using PSIM software. The feasibility of the proposed ZVS auxiliary circuit for PWM three level DC-DC Converter with PSIM (a commercially available software package dedicated for power electronic converter simulations) and proposed converter was simulated based on the following specifications:

The following components were used to implement the simulation of the proposed DC-DC converter:

TABLE I: PARAMETER SPECIFICATIONS.

PARAMETERS	SPECIFICATIONS
Auxiliary Inductor Lc	140µH
DC blocking Capacitor Cr	1µF
Variable Load Resistor R_o	10 – 400 Ω
Output Capacitor C_o	200 µF

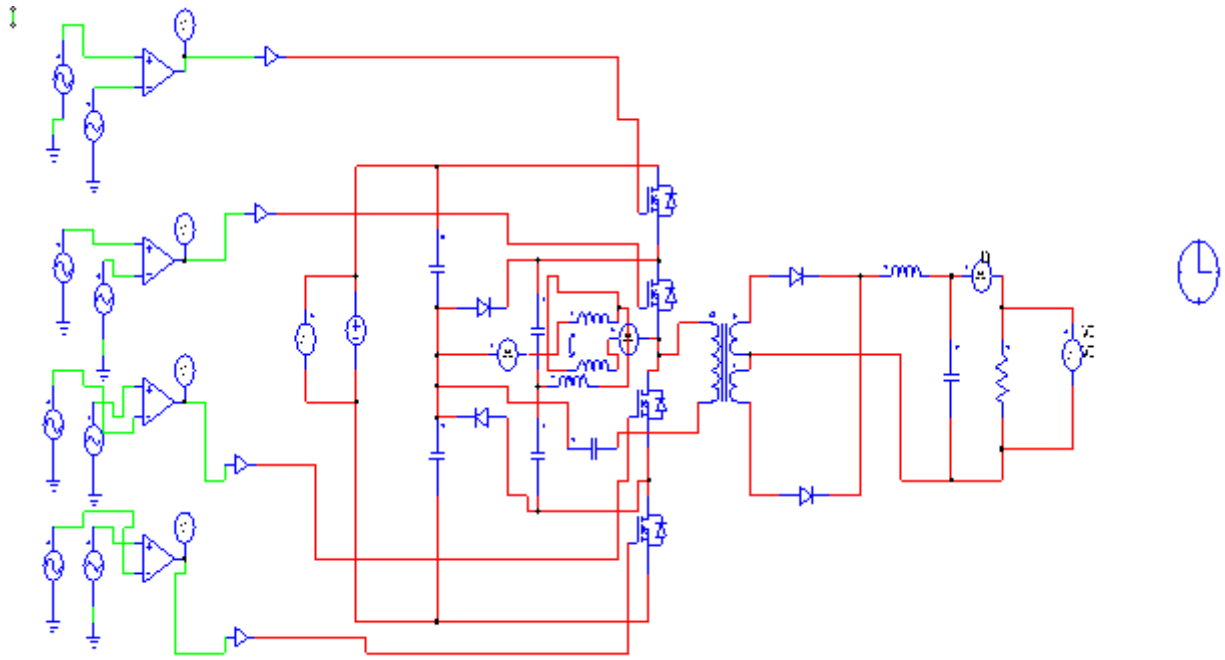

Figure 2.Simulation diagram of proposed system

PULSE GENERATOR WAVEFORMS

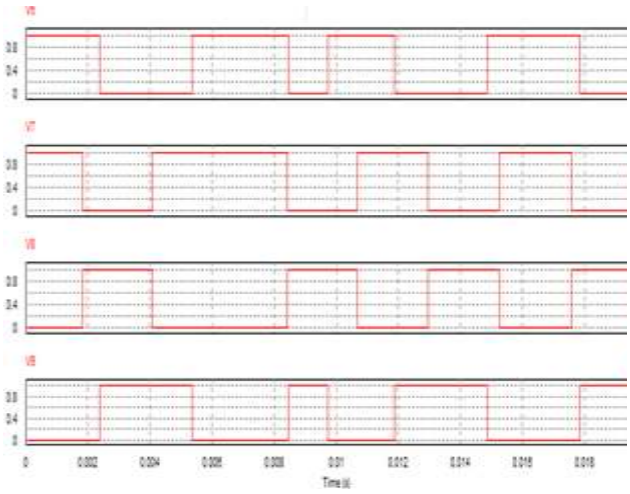

Figure 3.Gating signals of switch s1,s2,s3,s4.

Figure 3 demonstrates the simulated switching waveforms of proposed converter by PWM Pulse width modulation technique.

In PWM technique, the triangular wave is compared with the sine wave by using a comparator and the values of the Duty cycle and frequency should be given and based on this pulses will be generating.

In these waveforms gate pulse signals of the MOSFET switches S1 and S4 are complimentary and switches S2 and S3 are complimentary.

The switches S1,S2,S3,S4 can be turned off with ZVS. Once the switch's gate pulse signal has been removed then the switch S1,S2,S3,S4 are turned off simultaneously.

OUTPUT VOLTAGE WAVEFORM

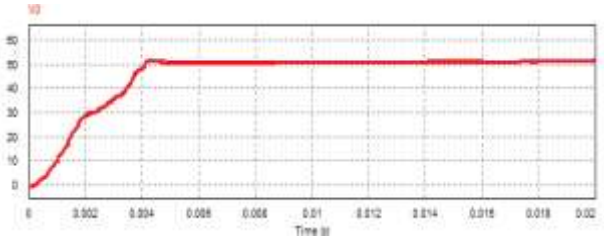

Figure 4.Output voltage waveform

The simulated output voltage of a dc-dc converter is found to be 51v dc and it can be shown in the figure 4.

OUTPUT CURRENT WAVEFORM

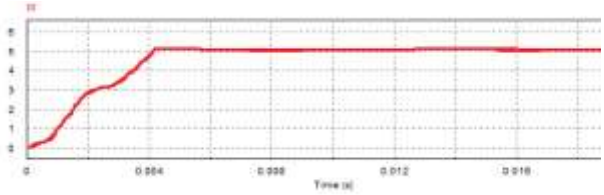

Figure 5.Output current waveform

The simulated output current of a dc-dc converter is found to be 5v dc, and it can be shown in figure 5 .

COUPLED INDUCTOR CURRENT WAVEFORM

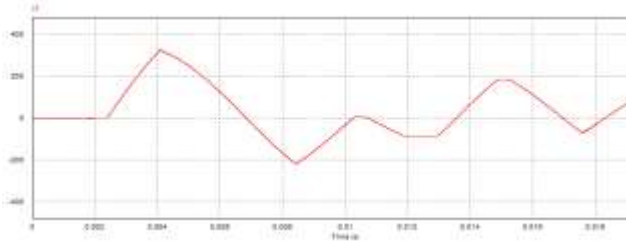

Figure 5.Coupled inductor current waveform

The simulated coupled inductor current waveform of a dc-dc converter can be shown in figure 5. The coupled inductor required will be AC in the sense that the ramp will be bipolar. So in this case, maximum volts-seconds during each half switching cycle is the key factor which should be considered for designing the inductor.

The value of this inductance should be the same as the value of the coupled inductor necessary for the largest value of the ramp current which occurs at no load operation of the converter. The output filter inductor should be made large at lower loads to satisfy the continuous operation. The value of the output inductor should be 1µH so that the inductor should be implemented with just one turn on the planer core. The duty ratio of the dc–dc three-level converter will increase with increasing output load because of the loss of effective duty cycle due to the existence of operation to overcome the losses in the converter and also whether the output inductor current will be in continuous or discontinuous mode . Especially at high loads, the currents in the transformer leakage inductor and the non-coupled auxiliary circuit can be large enough during turn-off of devices S1 or S4, which can result in abrupt charging of their output capacitances.

6. CONCLUSION

The new soft switching PWM DC-DC converter has been proposed. The zero voltage switching has been verified in the simulation results to ensure lower switching losses. The inherent properties of the dc-dc converter have been actually clarified from the simulation results as follows:

- High conversion efficiency over 95% can be achieved.
- A Wide range of soft switching ZVS operations can be attained.

Compared to the conventional method the proposed DC-DC Converter has higher efficiency and it satisfies the Energy Star Platinum Efficiency standard.

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